AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

What is claimed is:

1. (Previously presented) An interface for receiving data from an image sensor having an imaging array and a clock generator for transfer to a processor system comprising:
   - a memory for storing imaging array data and clocking signals at a rate determined by the clocking signals;
   - a signal generator for generating a signal for transmission to the processor system in response to the quantity of data in the memory; and
   - a circuit for controlling the transfer of the data from the memory at a rate determined by the processor system.

2. (Previously presented) An interface as claimed in claim 1 wherein the memory is a first-in first-out (FIFO) buffer.

3. (Previously presented) An interface as claimed in claim 2 wherein the signal generator generates an interrupt signal for transmission to the processor system.

4. (Previously presented) An interface as claimed in claim 3 wherein the circuit for controlling the transfer of the data includes:
   - a command decoder for receiving address and command signals from the processor system;

- a configuration register for storing configuration data for the FIFO buffer; and
- a read control for controlling the read-out of the FIFO buffer.

5. (Previously presented) An interface as claimed in claim 4 wherein the interface further includes an array register for determining the dimension of the imaging array data.

6. (Previously presented) An interface as claimed in claim 2 wherein the signal generator generates a bus request signal for transmission to a bus arbitration unit for the processor system.

7. (Previously presented) An interface as claimed in claim 6 wherein the circuit for controlling the transfer of the data further includes:
- a command decoder for receiving address and command signals from the processor system;
- a configuration register storing configuration data for the FIFO buffer;
- a read control for controlling the read-out of the FIFO buffer; and
- a bus command unit for receiving control of the system bus and providing an address for the data read-out from the FIFO buffer.

8. (Previously presented) An interface as claimed in claim 1 wherein the memory is an addressable memory.

9. (Previously presented) An interface as claimed in claim 8 wherein the signal generator generates an interrupt signal for transmission to the processor system.

10. (Previously presented) An interface as claimed in claim 9 wherein the circuit for controlling the transfer of the data includes:

- a command decoder for receiving address and command signals from the processor system;
- a configuration register for storing configuration data for the addressable memory; and
- a read control for controlling the read-out of the addressable memory.

11. (Previously presented) An interface as claimed in claim 10 wherein the interface further includes an array register for determining the dimension of the imaging array data.

12. (Previously presented) An interface as claimed in claim 8 wherein the signal generator generates a bus request signal for transmission to a bus arbitration unit for the processor system.

13. (Previously presented) An interface as claimed in claim 12 wherein the circuit for controlling the transfer of the data further includes:
- a command decoder for receiving address and command signals from the processor system;
- a configuration register storing configuration data for the addressable memory;
- a read control for controlling the read-out of the addressable memory; and
- a bus command unit for receiving control of the system bus and providing an address for the data read-out from the addressable memory.

14. (Previously presented) An interface as claimed in claim 13 wherein the interface further includes an array register for determining the dimension of the imaging array data.

15. (Cancelled)

16. (Currently amended) An integrated semiconductor imaging circuit ~~as claimed in claim 15 where the interface includes~~ for use with an electronic processing system having a data bus comprising:

- an imaging array sensor having an array of sensing pixels and an array address generator integrated on a die; and
- an interface integrated on the die for receiving data from the imaging array sensor as determined by the imaging array sensor and adapted to transfer the data to the electronic processing system as determined by the electronic processing system, the interface including:
  - a memory for storing imaging array data and address signals at a rate determined by the imaging array sensor; and
  - a circuit for controlling the transfer of the data from the memory to the data bus at a rate determined by the electronic processing system.

17. (Previously presented) An integrated semiconductor imaging circuit as claimed in claim 16 wherein the memory includes a first-in first-out (FIFO) buffer.

18. (Previously presented) An integrated semiconductor imaging circuit as claimed in claim 17 which further includes a bus arbitration unit coupled to the circuit for controlling the transfer of the data.

19. (Previously presented) An integrated semiconductor imaging circuit as claimed in claim 17 which further includes a bus arbitration unit integrated on the die and coupled to the circuit for controlling the transfer of the data.

20. (Previously presented) An integrated semiconductor imaging circuit as claimed in claim 16 wherein the memory includes an addressable memory.

21. (Previously presented) An integrated semiconductor imaging circuit as claimed in claim 20 which further includes a bus arbitration unit coupled to the circuit for controlling the transfer of the data.

22. (Previously presented) An integrated semiconductor imaging circuit as claimed in claim 20 which further includes a bus arbitration unit integrated on the die and coupled to the circuit for controlling the transfer of the data.

23-30. (Cancelled)